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UNIFIED DECODER ARCHITECTURE

RELATED APPLICATIONS

[0001] [Not Applicable]

FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] [Not Applicable]

[MICROFICHE/COPYRIGHT REFERENCE]

[0003] [Not Applicable]

BACKGROUND OF THE INVENTION

[0004] A number of different standards exist for encoding video data. In some cases, the video data is also compressed as part of the encoding process. For example, the Motion Pictures Expert Group (MPEG) has devised two such standards commonly known as MPEG-2, and Advanced Video Coding (MPEG-4). Another example of an encoding standard is known as the Digital Video-25 (DV-25).

[0005] The encoded video data is decoded by a video decoder. However, a video decoder can receive encoded video data that is encoded with any one of a wide variety of encoding standards. In order to display the video data, the video decoder needs to be able to determine and decode video data that is encoded with any one of the wide variety of encoding standards.

[0006] Although some video decoders are capable of decoding video data from multiple formats, the video decoders comprise special hardware dedicated to decoding

each one of the wide variety of encoding standards. This is disadvantageous because the additional hardware increases the cost of the decoder system.

[0007] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with embodiments presented in the remainder of the present application with references to the drawings.

BRIEF SUMMARY OF THE INVENTION

[0008] Presented herein is a unified decoder architecture.

[0009] In one embodiment, there is presented a system for decoding video data encoded with a particular standard. The system comprises a video decoder, instruction memory, and a host processor. The video decoder decodes the video data encoded with the particular standard. The instruction memory stores a first set of instructions and a second set of instructions. The first set of instructions are for decoding encoded video data according to a first encoding standard. The second set of instruction are for decoding encoded video data according to a second encoding standard. The host processor provides an indication to the video decoder indicating the particular encoding standard. The video decoder executes the first set of instructions if the indication indicates that the particular encoding standard is the first encoding standard and executes the second set of instructions if the indication indicates that the particular encoding standard is the second encoding standard.

[0010] In another embodiment, there is presented a method for decoding video data encoded with a particular standard. The method comprises providing an indication to a video decoder indicating the particular encoding standard to the video decoder, executing a first set of instructions if the indication indicates that the particular encoding standard is a first encoding standard, and executing a second set of instructions if the indication indicates that

the particular encoding standard is the second encoding standard.

[0011] In another embodiment, there is presented a system for decoding video data encoded with a particular standard. The system comprises a code memory and a processor. The code memory stores instructions. The processor loads the code memory with a first set of instructions for decoding encoded video data according to a first encoding standard, where the video data is encoded according to the first encoding standard and loads the code memory a second set of instruction for decoding encoded video data according to a second encoding standard, wherein the video data is encoded according to the second encoding standard.

[0012] These and other advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0013] **FIGURE 1** is a block diagram of an exemplary decoder system for decoding compressed video data, in accordance with an embodiment of the present invention;

[0014] **FIGURE 2** is a block diagram of a circuit for decoding encoded video data in accordance with an embodiment of the present invention;

[0015] **FIGURE 3** is a flow diagram for decoding compressed video data in accordance with an embodiment of the present invention; and

[0016] **FIGURE 4** is a block diagram of the video decoder in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring now to **FIGURE 1** there is illustrated a block diagram of an exemplary decoder system for decoding compressed video data, in accordance with an embodiment of the present invention. Data is received and stored in a presentation buffer 203 within a Synchronous Dynamic Random Access Memory (SDRAM) 201. The data can be received from either a communication channel or from a local memory, such as, for example, a hard disc or a DVD. In addition, the video data may be compressed using different encoding standards, such as, but not limited to, MPEG-2, DV-25, and MPEG-4.

[0018] The data output from the presentation buffer 203 is then passed to a data transport processor 205. The data transport processor 205 demultiplexes the transport stream into packetized elementary stream constituents, and passes the audio transport stream to an audio decoder 215 and the video transport stream to a video transport processor 207 and then to an MPEG video decoder 209. The audio data is then sent to the output blocks, and the video is sent to a display engine 211.

[0019] The display engine 211 scales the video picture, renders the graphics, and constructs the complete display. Once the display is ready to be presented, it is passed to a video encoder 213 where it is converted to analog video using an internal digital to analog converter (DAC). The digital audio is converted to analog in an audio digital to analog converter (DAC) 217.

[0020] The video decoder 209 can decode encoded video data that is encoded with any one of a plurality of

encoding standards. The video decoder 209 uses firmware to decode the encoded video data. A portion of the firmware can be used for decoding video data for each of the plurality of standards, while other portions are specific to a particular standard. Accordingly, the video decoder executes a combination of the portions of the firmware that are common for decoding each of the different standards and the portions that are unique to the specified standard used for encoding the encoded video data.

[0021] A host processor 290 detects the specific standard used for encoding the encoded video data and provides an indication indicating the specific standard to the video decoder 209. Responsive thereto, the video decoder 209 selects the portions of the firmware that are specific to the encoding standard for execution along with the portions that are common for all of the standards.

[0022] Referring now to **FIGURE 2**, there is illustrated a block diagram of a circuit for decoding encoded video data in accordance with an embodiment of the present invention. The circuit comprises a video decoder 209, a host processor 290, a first instruction memory 291, and a second instruction memory 292. The first instruction memory 291 stores firmware comprising a first plurality of instructions 295a that are common for decoding encoded video data encoded with any of a plurality of encoding standards, a second plurality of instructions 295b that is unique for decoding encoded video data encoded with a first encoding standard, a third plurality of instructions 295c that is unique for decoding encoded video data encoded with a second encoding standard, a fourth plurality of instructions 295d that is unique for decoding encoded video

data encoded with a third encoding standard. The first encoding standard can comprise, for example, MPEG-2. The second encoding standard can comprise, for example, DV-25. The third encoding standard can comprise, for example, MPEG-4. Although the pluralities of instructions 295a, 295b, 295c, 295d are indicated by continuous regions for ease of illustration, it is noted that the pluralities of instructions 295a, 295b, 295c, 295d do not necessarily occupy continuous regions of the first instruction memory 291.

[0023] The host processor 290 executes instructions stored in the second instruction memory 292. Execution of the instructions in the second instruction memory 292 cause the host processor 290 to detect the encoding standard used for encoding the compressed video data and provide an indicator indicating the encoding standard to the video decoder 209.

[0024] The video decoder 209 includes a control register 297 comprising a plurality of bits. The host processor 290 includes the encoding standard to the video decoder 209 by setting certain values in one or more of the bits in the control register. For example, in an exemplary case, the host processor 290 can set two bits from the control register 297 to indicate the encoding standard, wherein the values of the two bits indicate the encoding standard as set forth in the table below.

Bit Value	Encoding Standard
00	Not Used
01	MPEG-2
10	DV-25
11	MPEG-4

[0025] Based on the indicated encoding standard, the video decoder 209 selects and executes the portions of the firmware that are specific to the encoding standard for execution along with the portions that are common for the plurality of encoding standards.

[0026] Referring now to **FIGURE 3**, there is illustrated a flow diagram for decoding compressed video data in accordance with an embodiment of the present invention. At 305, the host processor 290 detects the encoding standard for encoding the encoded video data.

[0027] After determining the encoding standard for encoding the encoded video data, the host processor 290 provides (310) an indication indicating the encoding standard to the video decoder 209.

[0028] At 315, the video decoder 209 receives the indication indicating the encoding standard. At 320, a determination is made whether the encoding standard is a first encoding standard, a second encoding standard, or a third encoding standard.

[0029] If the encoding standard is a first encoding standard at 320, the video decoder 209 selects (325) the portions of the firmware that are unique to the first encoding standard. At 330, the video decoder 209 decodes the encoded video data by executing the portions of the firmware that are unique to the first encoding standard and the portions of the firmware that are common to all of the plurality of encoding standards.

[0030] If the encoding standard is a second encoding standard at 320, the video decoder 209 selects (335) the portions of the firmware that are unique to the second

encoding standard. At 340, the video decoder 209 decodes the encoded video data by executing the portions of the firmware that are unique to the second encoding standard and the portions of the firmware that are common to all of the plurality of encoding standards.

[0031] If the encoding standard is a third encoding standard at 320, the video decoder 209 selects (355) the portions of the firmware that are unique to the third encoding standard. At 360, the video decoder 209 decodes the encoded video data by executing the portions of the firmware that are unique to the third encoding standard and the portions of the firmware that are common to all of the plurality of encoding standards.

[0032] Referring now to **FIGURE 4**, there is illustrated a block diagram of an exemplary video decoder 209 in accordance with an embodiment of the present invention. The video decoder 209 comprises a master row engine 405 and a slave row engine 410. The master row engine 405 supports the MPEG-2, MPEG-4, and DV-25 encoding standards. However, in the case of MPEG-2 High Definition Television (HDTV), although the instructions are the same, the rate of data for decoding is high. Accordingly, the slave row engine 410 supplements the master row engine 405 for decoding MPEG-2 video data.

[0033] The host processor sends an indication to a master processor 430 in the master row engine 410, indicating the type of video data that is to be decoded. Responsive to receiving the signal, the master processor 430 loads the appropriate combination of instructions 295a, 295b, 295c, 295d from the instruction memory into a code data memory 425. **[[[or is it the host processor that loads**

the instructions??]]] If the indicator indicates that the video data is MPEG-2, the master processor 430 also loads the appropriate combination of instructions 295a, 295b, 295c, 295d from the instruction memory into a code data memory 550 in the slave row engine 410. After loading the appropriate combination of instructions 295a, 295b, 295c, 295d, the appropriate combination of instructions cause the master row engine 405 to accesses the video data with a video DMA 420.

[0034] The video data is received by a bitstream extractor 460. In the case where the video data is MPEG-2, the video data is also received by bitstream extractor 510. The combination of instructions 295a, 295b, 295c, 295d configure and otherwise drive the appropriate hardware in the master row engine 409 and slave row engine 410 for the type of video data received.

[0035] The master row engine 409 includes hardware components for decoding DV-25, MPEG-2, and MPEG-4 video. The master row engine 409 comprises a Video Engine Interface VEIF, a Quantizer Command Programming (QCP) First-In First-Out queue (FIFO) 490, a Motion Computer (MOTC) 440, a Video Request Manager (VREQM) FIFO 445, an Inverse Quantizer 525, a Video Request Manager 450, an Inverse Discrete Cosine Transformation (IDCT) block 500, and Pixel Reconstructor 455 that are used when decoding DV-25, MPEG-2, and MPEG-4 video data. The master row engine also includes a DV Inverse Quantizer (DVIQ) 480, a DV Variable Length Decoder (DV VLD) 465, and a DV IDCT Preprocessor 505 that are used when decoding DV-25 video data.

[0036] The slave row engine 410 comprises a master VLD 515, a slave VLD 520, video engine interface (VEIF) 525, a QCP FIFO 530, an inverse quantizer 535, an IDCT 540, a bridge 545, a slave processor 555, an MOTC 560, a VREQM FIFO 565, a video request manager 570, and a pixel reconstructer 575 that are used for decoding MPEG-2 video data.

[0037] One embodiment of the present invention may be implemented as a board level product, as a single chip, application specific integrated circuit (ASIC), or with varying levels integrated on a single chip with other portions of the system as separate components. The degree of integration of the system will primarily be determined by speed and cost considerations. Because of the sophisticated nature of modern processors, it is possible to utilize a commercially available processor, which may be implemented external to an ASIC implementation of the present system. Alternatively, if the processor is available as an ASIC core or logic block, then the commercially available processor can be implemented as part of an ASIC device with various functions implemented as firmware.

[0038] While the invention has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the invention. In addition, many modifications may be made to adapt particular situation or material to the teachings of the invention without departing from its scope. Therefore, it is intended that the invention not be limited to the particular embodiment(s) disclosed, but that

the invention will include all embodiments falling within the scope of the appended claims.